UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/712,229	11/12/2003	Andrew L. Van Brocklin	200309795-1	8482

22879 7590 06/27/2006

HEWLETT PACKARD COMPANY
P O BOX 272400, 3404 E. HARMONY ROAD
INTELLECTUAL PROPERTY ADMINISTRATION
FORT COLLINS, CO 80527-2400

EXAMINER	
DHARIA, PRABODH M	

ART UNIT	PAPER NUMBER
2629	

DATE MAILED: 06/27/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/712,229	VAN BROCKLIN ET AL.	
	Examiner	Art Unit	
	Prabodh M. Dharia	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *1* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 November 2003*.

2a)☐ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-44* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) _____ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☒ Claim(s) *1-44* are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *05-04-05,11-12-03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. **Status:** Please all the replies and correspondence should be addressed to examiner's new art unit 2629. Receipt is acknowledged of papers submitted on 11-12-2003 under application for patent, which have been placed of record in the file. Claims 1-44 are pending in this action.

Information Disclosure Statement

2. The information disclosure statement (IDS) submitted on 11-12-2003,05-04-2005 is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosures statement is being considered by the examiner.

Election/Restrictions

3. Restriction to one of the following inventions is required under 35 U.S.C. 121:

I. Claims 1-13 are drawn to a large area display, comprising: a pixel layer including display elements; a connection layer; drivers in communication with the pixel layer and the connection layer, the drivers configured for driving the display elements in the pixel layer and configured for communicating through the connection layer; and a laminate formed of the pixel layer, the connection layer and drivers the display elements comprises at least one of liquid crystal display

(LCD), light emitting diode (LED), organic LED (OLED), polymer light emitting device (PLED), electroluminescent (EL), electrophoretic display, electrochromic display, electrowetting, gas plasma and fiber plasma; classified in class 345, subclass 204.

II. Claims 14-18 are drawn to a large area display, comprising: a plurality of sub-displays, each of the plurality of sub-displays comprising: a display element layer for emitting light; a driver in communication with the display element layer and configured for driving pixels in the display element layer; and a connection layer in communication with the driver and configured for serial data routing; and wherein the plurality of sub-displays form a large area display; classified in class385 subclass 04.

III Claims 19-25 are drawn to a method of manufacturing a large area display, comprising: providing a pixel layer including a matrix of pixels; providing a connection layer; providing drivers; and laminating the pixel layer, the drivers and the connection layer together to form an operable large area display; a pixel layer comprises providing one of a liquid crystal display (LCD) pixel layer, a light emitting diode (LED) pixel layer, an organic LED (OLED) pixel layer, a polymer light emitting device (PLED) pixel layer, an electroluminescent (EL) pixel layer, an electrophoretic display layer, electrochromic display layer, electrowetting display layer, gas plasma display layer and a fiber plasma display layer; at least

one control device for each pixel comprises providing at least one metal insulator metal (MIM) device for each pixel; classified in class 349 subclass 42.

IV Claims 26-37 are drawn to A large area display comprising: a means for emitting light including an array of sub-arrays each sub-array including an array of pixels; a means for driving each array of pixels of each sub-array of the array of sub-arrays; and a means for communicating display data, sensing and testing signals to and from a data source to the means for driving the array of pixels; the means for emitting light comprises at least one of liquid crystal display (LCD), light emitting diode (LED), organic LED (OLED), polymer light emitting device (PLED), electroluminescent (EL), electrophoretic display, electrochromic display, electrowetting, gas plasma and fiber plasma; the complementary transistors comprise p-channel and n-channel amorphous or polycrystalline or single crystal silicon; the complementary transistors comprise n-channel organic semiconductor paired with p-channel polycrystalline silicon; classified in class 348 subclass 46.

V Claims 38-44 are drawn to an apparatus for manufacturing a large area display, comprising: a means for providing a pixel layer; a means for providing drivers; a means for providing a connection layer; and a means for laminating the pixel layer, drivers and connection layer together to form an operable large area display; a means for placing features on the pixel layer or the connection layer; a features comprises an embossing roller with patterning; low-temperature

polysilicon (LTPS) technology; and amorphous crystal growing (CG silicon) technology; the means for laminating the pixel layer, drivers and connection layer to form an operable large area display comprises roll-to-roll; classified in class 313 subclass 503.

4. The inventions are distinct from each other because:

Invention I relates to; a large area display, comprising: a pixel layer including display elements; a connection layer; drivers in communication with the pixel layer and the connection layer, the drivers configured for driving the display elements in the pixel layer and configured for communicating through the connection layer; and a laminate formed of the pixel layer, the connection layer and drivers the display elements comprises at least one of liquid crystal display (LCD), light emitting diode (LED), organic LED (OLED), polymer light emitting device (PLED), electroluminescent (EL), electrophoretic display, electrochromic display, electrowetting, gas plasma and fiber plasma; however, it does not relate to a large area display, comprising: a plurality of sub-displays, each of the plurality of sub-displays comprising: a display element layer for emitting light; a driver in communication with the display element layer and configured for driving pixels in the display element layer; and a connection layer in communication with the driver and configured for serial data routing; and wherein the plurality of sub-displays form a large area display; a large area display, comprising: providing a pixel layer including a matrix of pixels; providing a connection layer; providing drivers; and laminating the pixel layer, the drivers and the connection layer together to form an operable large area display; a pixel layer comprises providing one of a liquid crystal display (LCD) pixel layer,

a light emitting diode (LED) pixel layer, an organic LED (OLED) pixel layer, a polymer light emitting device (PLED) pixel layer, an electroluminescent (EL) pixel layer, an electrophoretic display layer, electrochromic display layer, electrowetting display layer, gas plasma display layer and a fiber plasma display layer; at least one control device for each pixel comprises providing at least one metal insulator metal (MIM) device for each pixel; A large area display comprising: a means for emitting light including an array of sub-arrays each sub-array including an array of pixels; a means for driving each array of pixels of each sub-array of the array of sub-arrays; and a means for communicating display data, sensing and testing signals to and from a data source to the means for driving the array of pixels; the means for emitting light comprises at least one of liquid crystal display (LCD), light emitting diode (LED), organic LED (OLED), polymer light emitting device (PLED), electroluminescent (EL), electrophoretic display, electrochromic display, electrowetting, gas plasma and fiber plasma; the complementary transistors comprise p-channel and n-channel amorphous or polycrystalline or single crystal silicon; the complementary transistors comprise n-channel organic semiconductor paired with p-channel polycrystalline silicon; and an apparatus for manufacturing a large area display, comprising: a means for providing a pixel layer; a means for providing drivers; a means for providing a connection layer; and a means for laminating the pixel layer, drivers and connection layer together to form an operable large area display; a means for placing features on the pixel layer or the connection layer; a features comprises an embossing roller with patterning; low-temperature polysilicon (LTPS) technology; and amorphous crystal growing (CG silicon) technology; the means for laminating the pixel layer, drivers and connection layer to form an operable large area display comprises roll-to-roll.

Invention II relates relate to a large area display, comprising: a plurality of sub-displays, each of the plurality of sub-displays comprising: a display element layer for emitting light; a driver in communication with the display element layer and configured for driving pixels in the display element layer; and a connection layer in communication with the driver and configured for serial data routing; and wherein the plurality of sub-displays form a large area display; however, it does not relate to a large area display, comprising: a pixel layer including display elements; a connection layer; drivers in communication with the pixel layer and the connection layer, the drivers configured for driving the display elements in the pixel layer and configured for communicating through the connection layer; and a laminate formed of the pixel layer, the connection layer and drivers the display elements comprises at least one of liquid crystal display (LCD), light emitting diode (LED), organic LED (OLED), polymer light emitting device (PLED), electroluminescent (EL), electrophoretic display, electrochromic display, electrowetting, gas plasma and fiber plasma; a large area display, comprising: providing a pixel layer including a matrix of pixels; providing a connection layer; providing drivers; and laminating the pixel layer, the drivers and the connection layer together to form an operable large area display; a pixel layer comprises providing one of a liquid crystal display (LCD) pixel layer, a light emitting diode (LED) pixel layer, an organic LED (OLED) pixel layer, a polymer light emitting device (PLED) pixel layer, an electroluminescent (EL) pixel layer, an electrophoretic display layer, electrochromic display layer, electrowetting display layer, gas plasma display layer and a fiber plasma display layer; at least one control device for each pixel comprises providing at least one metal insulator metal (MIM) device for each pixel; a large area display comprising: a means for emitting light including an array of sub-arrays each sub-array including an array of

pixels; a means for driving each array of pixels of each sub-array of the array of sub-arrays; and a means for communicating display data, sensing and testing signals to and from a data source to the means for driving the array of pixels; the means for emitting light comprises at least one of liquid crystal display (LCD), light emitting diode (LED), organic LED (OLED), polymer light emitting device (PLED), electroluminescent (EL), electrophoretic display, electrochromic display, electrowetting, gas plasma and fiber plasma; the complementary transistors comprise p-channel and n-channel amorphous or polycrystalline or single crystal silicon; the complementary transistors comprise n-channel organic semiconductor paired with p-channel polycrystalline silicon; and a large area display, comprising: a means for providing a pixel layer; a means for providing drivers; a means for providing a connection layer; and a means for laminating the pixel layer, drivers and connection layer together to form an operable large area display; a means for placing features on the pixel layer or the connection layer; a features comprises an embossing roller with patterning; low-temperature polysilicon (LTPS) technology; and amorphous crystal growing (CG silicon) technology; the means for laminating the pixel layer, drivers and connection layer to form an operable large area display comprises roll-to-roll.

Invention III relates to a large area display, comprising: providing a pixel layer including a matrix of pixels; providing a connection layer; providing drivers; and laminating the pixel layer, the drivers and the connection layer together to form an operable large area display; a pixel layer comprises providing one of a liquid crystal display (LCD) pixel layer, a light emitting diode (LED) pixel layer, an organic LED (OLED) pixel layer, a polymer light emitting device (PLED) pixel layer, an electroluminescent (EL) pixel layer, an electrophoretic display layer,

electrochromic display layer, electrowetting display layer, gas plasma display layer and a fiber plasma display layer; at least one control device for each pixel comprises providing at least one metal insulator metal (MIM) device for each pixel; however, it does not relate to large area display, comprising: a pixel layer including display elements; a connection layer; drivers in communication with the pixel layer and the connection layer, the drivers configured for driving the display elements in the pixel layer and configured for communicating through the connection layer; and a laminate formed of the pixel layer, the connection layer and drivers the display elements comprises at least one of liquid crystal display (LCD), light emitting diode (LED), organic LED (OLED), polymer light emitting device (PLED), electroluminescent (EL), electrophoretic display, electrochromic display, electrowetting, gas plasma and fiber plasma; a large area display, comprising: a plurality of sub-displays, each of the plurality of sub-displays comprising: a display element layer for emitting light; a driver in communication with the display element layer and configured for driving pixels in the display element layer; and a connection layer in communication with the driver and configured for serial data routing; and wherein the plurality of sub-displays form a large area display; a large area display comprising: a means for emitting light including an array of sub-arrays each sub-array including an array of pixels; a means for driving each array of pixels of each sub-array of the array of sub-arrays; and a means for communicating display data, sensing and testing signals to and from a data source to the means for driving the array of pixels; the means for emitting light comprises at least one of liquid crystal display (LCD), light emitting diode (LED), organic LED (OLED), polymer light emitting device (PLED), electroluminescent (EL), electrophoretic display, electrochromic display, electrowetting, gas plasma and fiber plasma; the complementary transistors comprise p-

channel and n-channel amorphous or polycrystalline or single crystal silicon; the complementary transistors comprise n-channel organic semiconductor paired with p-channel polycrystalline silicon; and a large area display, comprising: a means for providing a pixel layer; a means for providing drivers; a means for providing a connection layer; and a means for laminating the pixel layer, drivers and connection layer together to form an operable large area display; a means for placing features on the pixel layer or the connection layer; a features comprises an embossing roller with patterning; low-temperature polysilicon (LTPS) technology; and amorphous crystal growing (CG silicon) technology; the means for laminating the pixel layer, drivers and connection layer to form an operable large area display comprises roll-to-roll.

Invention IV relates to a large area display comprising: a means for emitting light including an array of sub-arrays each sub-array including an array of pixels; a means for driving each array of pixels of each sub-array of the array of sub-arrays; and a means for communicating display data, sensing and testing signals to and from a data source to the means for driving the array of pixels; the means for emitting light comprises at least one of liquid crystal display (LCD), light emitting diode (LED), organic LED (OLED), polymer light emitting device (PLED), electroluminescent (EL), electrophoretic display, electrochromic display, electrowetting, gas plasma and fiber plasma; the complementary transistors comprise p-channel and n-channel amorphous or polycrystalline or single crystal silicon; the complementary transistors comprise n-channel organic semiconductor paired with p-channel polycrystalline silicon; however, it does not relate to a large area display, comprising: a pixel layer including display elements; a connection layer; drivers in communication with the pixel layer and the

connection layer, the drivers configured for driving the display elements in the pixel layer and configured for communicating through the connection layer; and a laminate formed of the pixel layer, the connection layer and drivers the display elements comprises at least one of liquid crystal display (LCD), light emitting diode (LED), organic LED (OLED), polymer light emitting device (PLED), electroluminescent (EL), electrophoretic display, electrochromic display, electrowetting, gas plasma and fiber plasma; a large area display, comprising: a plurality of sub-displays, each of the plurality of sub-displays comprising: a display element layer for emitting light; a driver in communication with the display element layer and configured for driving pixels in the display element layer; and a connection layer in communication with the driver and configured for serial data routing; and wherein the plurality of sub-displays form a large area display; a large area display, comprising: providing a pixel layer including a matrix of pixels; providing a connection layer; providing drivers; and laminating the pixel layer, the drivers and the connection layer together to form an operable large area display; a pixel layer comprises providing one of a liquid crystal display (LCD) pixel layer, a light emitting diode (LED) pixel layer, an organic LED (OLED) pixel layer, a polymer light emitting device (PLED) pixel layer, an electroluminescent (EL) pixel layer, an electrophoretic display layer, electrochromic display layer, electrowetting display layer, gas plasma display layer and a fiber plasma display layer; at least one control device for each pixel comprises providing at least one metal insulator metal (MIM) device for each pixel; and a large area display, comprising: a means for providing a pixel layer; a means for providing drivers; a means for providing a connection layer; and a means for laminating the pixel layer, drivers and connection layer together to form an operable large area display; a means for placing features on the pixel layer or the connection layer; a features

comprises an embossing roller with patterning; low-temperature polysilicon (LTPS) technology; and amorphous crystal growing (CG silicon) technology; the means for laminating the pixel layer, drivers and connection layer to form an operable large area display comprises roll-to-roll.

Invention V relates to a large area display, comprising: a means for providing a pixel layer; a means for providing drivers; a means for providing a connection layer; and a means for laminating the pixel layer, drivers and connection layer together to form an operable large area display; a means for placing features on the pixel layer or the connection layer; a features comprises an embossing roller with patterning; low-temperature polysilicon (LTPS) technology; and amorphous crystal growing (CG silicon) technology; the means for laminating the pixel layer, drivers and connection layer to form an operable large area display comprises roll-to-roll; and however, it does not relate to a large area display, comprising: a pixel layer including display elements; a connection layer; drivers in communication with the pixel layer and the connection layer, the drivers configured for driving the display elements in the pixel layer and configured for communicating through the connection layer; and a laminate formed of the pixel layer, the connection layer and drivers the display elements comprises at least one of liquid crystal display (LCD), light emitting diode (LED), organic LED (OLED), polymer light emitting device (PLED), electroluminescent (EL), electrophoretic display, electrochromic display, electrowetting, gas plasma and fiber plasma; a large area display, comprising: a plurality of sub-displays, each of the plurality of sub-displays comprising: a display element layer for emitting light; a driver in communication with the display element layer and configured for driving pixels in the display element layer; and a connection layer in communication with the driver and

configured for serial data routing; and wherein the plurality of sub-displays form a large area display; a large area display, comprising: providing a pixel layer including a matrix of pixels; providing a connection layer; providing drivers; and laminating the pixel layer, the drivers and the connection layer together to form an operable large area display; a pixel layer comprises providing one of a liquid crystal display (LCD) pixel layer, a light emitting diode (LED) pixel layer, an organic LED (OLED) pixel layer, a polymer light emitting device (PLED) pixel layer, an electroluminescent (EL) pixel layer, an electrophoretic display layer, electrochromic display layer, electrowetting display layer, gas plasma display layer and a fiber plasma display layer; at least one control device for each pixel comprises providing at least one metal insulator metal (MIM) device for each pixel; and a large area display comprising: a means for emitting light including an array of sub-arrays each sub-array including an array of pixels; a means for driving each array of pixels of each sub-array of the array of sub-arrays; and a means for communicating display data, sensing and testing signals to and from a data source to the means for driving the array of pixels; the means for emitting light comprises at least one of liquid crystal display (LCD), light emitting diode (LED), organic LED (OLED), polymer light emitting device (PLED), electroluminescent (EL), electrophoretic display, electrochromic display, electrowetting, gas plasma and fiber plasma; the complementary transistors comprise p-channel and n-channel amorphous or polycrystalline or single crystal silicon; the complementary transistors comprise n-channel organic semiconductor paired with p-channel polycrystalline silicon.

5. These above-mentioned reasons the inventions described and categorized by class /subclass above are distinct. Search required for each class and subclass is independent.

6. Because these inventions are distinct for the reasons given above and have acquired a separate status in the art as shown by their different classification, restriction for examination purposes as indicated is proper.

7. Applicant is advised that the reply to this requirement to be complete must include an election of the invention to be examined even though the requirement is traversed (37 CFR 1.143).

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Prabodh M. Dharia whose telephone number is 571-272-7668. The examiner can normally be reached on M-F 8AM to 5PM.

9. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

10. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished

applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

PD

AU2629

June 04,2006

BIPIN SHALWALA
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600